Amendments to the Specification:

Please replace the paragraph beginning on page 1, line 3 with the following rewritten paragraph:

This application is a continuation of U.S. Patent Application No. 09/498,779, now U.S. Patent No. 6,741,664 B1, and entitled "Low-Latency High-Speed Trellis Decoder", filed on February 5, 2000, which claims priority to U.S. Provisional Application No. 60/118,725 entitled "Ungerboeck Decoder Architecture" filed on February 5, 1999. These applications are expressly incorporated herein by reference as though fully set forth in full.

Please replace the paragraph beginning on page 3, line 15 with the following rewritten paragraph:

FIG. 8 is a block diagram of an embodiment of the butterfly circuit 604 or 608 of FIG. 6.~~5.~~

Please replace the paragraph beginning on page 4, line 19 with the following rewritten paragraph:

FIG. 1 illustrates an exemplary encoder 100 constructed in accordance with the ATSC Digital Television standard. The encoder 100 is represented in simplified form an interference filter pre-coder 101, and a trellis encoder 102 in combination with a signal mapper 104. The trellis encoder 102 includes a 4-state convolutional encoder 103. Data X_2 is pre-coded by the interference filter pre-coder 101 to produce data Y_2. Data Y_1 and

Y_2 are introduced unchanged to the signal mapper 104 as data Z_1 and Z_2. The data bit stream Y_1 is also inputted into the convolutional encoder 103, implemented as a linear feedback shift register, in order to generate a redundancy bit Z_0 ~~Which~~which is a necessary condition for the provision of the coding gain of the code. The signal mapper 104 maps the three bits $Z_0Z_1Z_2$ to one of the 8 signal values {-7, -5, -3, -1, 1, 3, 5, 7}, as indicated in FIG. 1.

Please replace the paragraph beginning on page 5, line 12 with the following rewritten paragraph:

FIG. 3 shows the trellis diagram for the trellis code specified in the ATSC Digital Television Standard and described in FIG. 1. In the trellis diagram, each vertical column of nodes represents the possible states that the encoder 100 (FIG. 1) can assume at a point in time. It is noted that the states of the encoder 100 are dictated by the states of the convolutional encoder 103 (FIG. 1). Since the convolutional encoder 103 has 2 delay elements, there are 4 distinct states. The 4 distinct states of the encoder 100 are identified by numerals 0 through 3. Successive columns of nodes represent the possible states of the convolutional encoder 103 at successive points in time.

Please replace the paragraph beginning on page 13, line 27 through page 14, line 2 with the following rewritten paragraph:

Similarly, the butterfly circuit 608 computes the new node metrics for states 2 and 3 based on the previous node metrics of states 1 and 3 provided by the circular buffers 606 and 602,

respectively. The butterfly circuit 608 then~~,~~ outputs the optimal trellis transitions (from predecessor states 1 and 3 to states2 and 3) and the new node metrics for states 2 and 3. The circular buffers 606 and 602 store the new node metrics for states 2 and 3, respectively, for the next computations.

Please replace the two paragraphs beginning on page 15, line 10, through page 16, line 2 with the following rewritten paragraph:

The branch metric 818 is added to the node metric 824 via adder 806 to produce a possible node metric 832. The branch metric 820 is added to the node metric 822 via adder 808 to produce a possible node metric 834. The comparator 812 outputs values of the possible node metrics to the multiplexer 816. The comparator 812 compares the two possible node metrics 832, 834. If metric 834 is greater than metric 832 then a 1 is outputted as a node transition. This bit value 1 will also cause the multiplexer 816 to select the value of node metric 832, which is the smaller of the possible node metrics 832, 834, to output as the new node metric of the successor state corresponding to this half of the butterfly circuit. For example, referring to the trellis diagram of FIG. 3, if the other half of the butterfly circuit is used for computing the new node metric for state 0 from predecessor states 0 and 2, then this half of the butterfly circuit is used for computing the new node metric of successor state 1 from the predecessor states_0 and 2. Then, the new node metric 836 is for successor state 1.

FIG. 9 is a diagram of an embodiment of the comparators used for comparing node metrics, such as the ones in the

butterfly circuit of FIG. 8. As discussed previously, to correctly compare the node metrics, the modulo-power- of-2 comparator needs to have one additional bit to the number of bits required to represent the maximum spread between any two of the node metrics. Thus,~~20~~ the comparator 900 is an N-bit comparator if the maximum spread can be represented by N-1 bits. The comparator 900 includes a (N-1)-bit comparator 902 and an exclusive-OR gate 904. The comparator 900 compares the last N-1 bits of node metric A with the last N-1 bits of node metric B. If the value represented by the last N-1 bits of A is greater than the one represented by the last N-1 bits of B, then comparator 902 outputs a 1. This 1 is exclusive-ORed with the most significant bits of A and B. The output of the exclusive-OR gate 904 is 1 if A is greater than B, and 0 if A is smaller than B.